

Application Number 10/687,084
Amendment dated November 19, 2004

Amendments to the Abstract of the Disclosure

Please replace the paragraph at page 27, lines 2 through 18 with the following amended paragraph:

The present invention discloses a layout method of a comparator array of a flash type analog to digital converting circuit. The flash type analog to digital converting circuit includes a reference voltage for generating $(2^n - 1)$ voltages and being arranged to be folded; a comparator array including $(2^n - 1)$ comparators for comparing voltage differences between the respective $(2^n - 1)$ number of voltages and an analog input signal to generate a digital thermometer code signal having $(2^n - 1)$ bits thermometer codes; and an encoder for encoding the digital thermometer code signal having $(2^n - 1)$ bits thermometer codes to generate an n-bit digital signal. The layout method of the flash type analog to digital converting circuit comprises arranging the comparators such that the comparators of $(2^n - 1)^{th}$ comparator to $(2^n/2)^{th}$ comparator are arranged in order and the comparators of $(2^n/2 - 1)^{th}$ comparator to a first comparator are arranged in reverse fashion between the comparators of the $(2^n - 1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator; and arranging the comparators such that the neighboring comparators adjacent to the respective $(2^n - 1)$ number of comparators remain at transit to the same state when the $(2^n - 1)^{th}$ comparator to the $(2^n/2)^{th}$ comparator transit to different states respectively. Therefore, increasing of an offset voltage due to the effects of the neighboring comparators is prevented without increasing a layout area size.